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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,387	12/04/2003	Kevin L. Robinson	LMC-34	7745

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2892	

MAIL DATE	DELIVERY MODE
03/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,387	ROBINSON, KEVIN L.	
	Examiner	Art Unit	
	Chuong A. Luu	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1 and 2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 5-19* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 3-19 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 3 and 5-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tserng et al. (U.S. 6,2787,826) in view of Igarashi et al. (U.S. 6,274,893).

Tserng discloses a heterostructure field effect transistor with

(3); (10) a first block comprising an enhancement mode PHEMT transistor on a substrate;

a second block comprising a depletion mode PHEMT transistor on the substrate, the second block operatively connected to the first block (see column 5, lines 15-31. Figure 1);

(7) an analog to digital converter, comprising an enhancement mode PHEMT device, a depletion mode PHEMT device on a single substrate (see column 6, lines 12-39. Figures 2-3);

(8) wherein the substrate comprises a group III-V element (see column 6, lines 64-65);

(9) wherein the substrate comprises gallium arsenide (see column 6, lines 64-65);

(11) wherein the plurality of integrated circuits can be interconnected to form a plurality of functional blocks which can be interconnected to create an operational electronic device (see Figure 1);

(12) wherein each of said PHEMT transistors comprises a recess defined in said substrate and a gate formed in said recess (see Figure 1);

(13) wherein the recess of the depletion mode PHEMT transistor is a single recess (see Figure 1);

(15) wherein the recess of the enhancement mode PHEMT transistor is a single recess (see Figure 1);

(16) wherein the recess of the depletion mode PHEMT transistor is a single recess, and each of said recesses is defined through at least one common layer of said substrate (see Figure 1).

Tserng teaches everything above except for a third block comprising a power PHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block; wherein the recess of the power PHEMT

transistor is a double recess; wherein the recess of the power PHEMT transistor is a double recess; wherein at least one of said gates is a T-gate; wherein a pinch off voltage of the depletion-mode PHEMT transistor is about positive 0.1 volts; and wherein a pinch off voltage of the enhancement-mode PHEMT transistor is about negative 1.0 volts and wherein the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC); wherein the circuit is a circuit capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies. However, Kim discloses a high electron mobility transistor with **(3); (7)...** a third block comprising a power PHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block; an analog input in communication with at least one of the first block, the second block (see column 18, lines 49-62. Figures 14H-14K); **(14); (16)** wherein the recess of the power PHEMT transistor is a double recess; **(17)** wherein at least one of said gates is a T-gate (see Figures 14H-14K). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teaching of Tserng and Kim to form a transistor since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8. Doing so would facilitate the manufacture of the semiconductor device and enhance the performance of the semiconductor transistor.

Even through, Tserng and Igarashi do not explicitly describe the at least one of said gates is a T-gate; wherein a pinch off voltage of the depletion-mode PHEMT

transistor is about positive 0.1 volts; and wherein a pinch off voltage of the enhancement-mode PHEMT transistor is about negative 1.0 volts and wherein the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC); wherein the circuit is a circuit capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies. However, the at least one of said gates is a T-gate; wherein a pinch off voltage of the depletion-mode PHEMT transistor is about positive 0.1 volts; and wherein a pinch off voltage of the enhancement-mode PHEMT transistor is about negative 1.0 volts and wherein the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC); wherein the circuit is a circuit capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies are considered to be obvious. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teaching of Tserng (accordance with the teaching of Igarashi) since it has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed and also it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. In re Aller, 105 USPQ 233 (see MPEP 2144.05). St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:30-3:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong A Luu/
Primary Examiner, Art Unit 2892
March 05, 2008